K17U 2006

Reg. No. : .....

Name : .....

III Semester B.C.A. Degree (CBCSS – Reg./Sup./Imp.) Examination, November 2017
(2014 Admn. Onwards)
Core Course
3B06BCA : COMPUTER ORGANIZATION

Time : 3 Hours Max. Marks : 40

SECTION – A

1. **One** word answer : (8×½=4)

   a) Common clock in the synchronous bus case is replaced by two timing control lines _____ and _____.

   b) Any condition that causes a pipeline to stall is called a _____

   c) _____ is measured by the rate at which instruction execution is completed.

   d) The compiler can reorder the instructions to perform some useful work during the _____

   e) Inter-Instruction Level and Intra-Instruction Level are the level of _____

   f) In _____ only one instruction stream is being acted on by the CPU during any one clock cycle.

   g) Each element in a vector is a _____

   h) The clock period should be long enough to let the _____

SECTION – B

Write short notes on **any seven** of the following questions : (7×2=14)

2. What is the significance of addressing mode ? Explain any one addressing mode.

3. What is Processor Status Register ?

4. Explain straight-line sequencing of instruction execution.

P.T.O.

5. Explain Three-state bus buffers.
6. Explain different instruction code formats.
7. What is privileged instructions ?
8. What is control word ?
9. What is I/O mapped I/O ?
10. Write short notes on Hit Rate and Miss Penalty.
11. What is an TLB ?

SECTION – C

Answer **any four** of the following questions : **(4×3=12)**

12. Explain I/O interface with the help of diagram.
13. What are Microinstructions ?
14. Explain vectored interrupt.
15. What is Fast Page Mode RAM ?
16. Distinguish between EPROM and EEPROM.
17. Explain 2's complement addition with an example.

SECTION – D

Write an essay on **any two** of the following questions : **(2×5=10)**

18. With the help of a diagram explain Associative Memory mapping.
19. Explain Hardwired Control Unit.
20. Explain supercomputers in detail.
21. Give an account of bus arbitration.